REMARKS

The disclosure was objected to because there was no Brief Description of Fig. 17. The Brief Description has been amended to include a description of Fig. 17.

Claims 14-25 and 29-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art ("APA") in view of U.S. Patent No. 6,020,616 to Bothra et al ("Bothra") and Japanese Pat. No. 9-289251 ("Japanese Patent").

The Examiner stated that Bothra teaches dummy gates having a predetermined length and width between ones of the transistors "**at a substantially identical gap between adjacent ones of the dummy gates . . .**" November 21, 2001 Office Action. [Emphasis added]. However, Bothra seems to suggest precisely the opposite. According to Bothra, "The plurality of dummy active regions are separated from the plurality of active regions by at least a bloat distance." Col. 3, lines 13-15. The bloat distance, as defined by Bothra is between 2 microns and 25 microns. *See* col. 6, lines 6-9. Therefore, the gap between a dummy and active gate can be anywhere from 2-25 microns. Indeed, by expressly teaching a bloat distance between dummy and active regions, Bothra teaches away from Applicant's invention. As such, Applicant's invention is not obvious in view of the applied references.

Claims 14-25 and 29-39 were also rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Pat. No. 9-289251. Claims 14, 18, 22, 29, 33 and 36 have been amended to clarify that adjacent transistor gates and adjacent dummy gates are located next to each other respectively, without intervening gates therebetween. Thus, it is clear that Applicant's invention is not rendered obvious by the Japanese patent.

For the foregoing reasons, reconsideration and allowance of claims 14-25 and 29-39 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 5, following the brief description of Fig.16 (which we added in our Response to the Office Action dated March 28, 2001) please further add:

Fig. 17 illustrates a power voltage applying line and a grounding voltage applying line.

IN THE CLAIMS

14. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially identical gap between ones of the adjacent transistor gates, without intervening transistor gates therebetween, on the substrate; and

a plurality of dummy gates having predetermined width and length between ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates, without intervening dummy gates therebetween, as that between the adjacent ones of the transistor gates on the substrate.

18. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially identical gap between adjacent ones of the transistor gates, without intervening transistor gates therebetween, on the substrate; and

a plurality of dummy gates having predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates, without intervening dummy gates therebetween, as that between the adjacent ones of transistor gates on the substrate.

22. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially identical gap between ones of the adjacent gates, without intervening transistor gates therebetween, on the substrate; and

a plurality of dummy gates having predetermined width and length outside ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates, without intervening dummy gates therebetween, as that between the adjacent ones of the transistor gates on the substrate.

29. (Amended) A semiconductor device comprising:

a substrate;

active regions having a source region and a drain region on the substrate;

a portion other than the active region on the substrate;

a plurality of transistor gates formed on the active regions, the gates being disposed between the source region and the drain region and having a first gap between adjacent gates, without intervening transistor gates therebetween;

a plurality of dummy gates formed on the portion, the dummy gates being characterized by a second gap between adjacent dummy gates, without intervening dummy gates therebetween;

wherein the second gap is substantially identical to the first gap.

33. (Amended) A semiconductor device comprising

a substrate;

a first region having a plurality of first active regions each having a source region and a drain region respectively and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region respectively and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first gates being

characterized by a first gap between neighboring transistor gates, without intervening transistor gates therebetween;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second gates also being characterized by the first gap between neighboring gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring dummy gates, without intervening dummy gates therebetween;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring dummy gates;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

36. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, without intervening transistors therebetween, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of transistor gates being characterized by a predetermined first dimension and a variable second dimension on the substrate; and

a plurality of dummy gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of dummy gates being characterized by dummy gates that substantially fill the region on the substrate devoid of transistor gates in the second dimension;

wherein the plurality of transistor gates have substantially identical first and second dimensions.